

Rita-51J

User's Guide

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1 INTRODUCTION

1.1 Overview

RITA (Rigel's Internet Technology Architecture) is a set of hardware and software components to facilitate placing very low cost controller nodes on the Internet or a private network, such as a company intranet or a personal home network. RITA is a flexible and extensible open architecture. RITA is an outgrowth of custom Internet controllers built by Rigel Corporation for industrial OEM customers, now being offered to the public as commercial off-the-shelf (COTS) units. Refer to the article "The RITA Philosophy" at www.rigelcorp.com for more information about RITA.

1.2 Hardware Overview

Rita-51J is the newest board in Rigel Corporation's line of RITA controllers. Rita-51J is a two-layer board intended for Internet and intranet applications. The board may be populated with a wide range of high-speed 8051 microcontrollers in the 44-pin PLCC package. The board uses the CS8900A to directly connect to a 10Base-T network using an RJ-45 connector. The MCS-51 / CS8900A combination takes advantage of readily available hardware and software tools as well as the wealth of publicly available applications source code.

The Rita-51J has one RS-232 serial port (two when populated with the DS87C520 or DS89C420). The board comes with 128K RAM and 128K 5-volt FLASH ROM. The Rita-51 Utility Software used to program the FLASH ROM is free with the board. The FLASH programming and erase operations can also be carried out from [Reads51](#). Rita-51J's small size makes it suitable for OEM applications. Its low cost and open architecture makes it a good choice for classroom instruction and hobbyists. It contains large memory

to facilitate embedded TCP/IP applications. In addition, Rita-51J contains a prototyping area, 4 user's buttons and 4 indicators, which make it an ideal test and development platform.

- Uses any 8051 in the 44 pin PLCC package
- 128K of SRAM
- 128K 5-volt FLASH ROM
- 1 full-duplex serial port on board (2 with the DS87C520 or the DS89C420)
- 12 general purpose digital input / output bits
- Demultiplexed processor Address and Data lines
- All system signals are available on a 40-pin header
- DS2502E48 device to provide a unique MAC (Ethernet) address
- Prototyping area for additional circuitry
- Shielded RJ-45 connector with LAN and LINK indicators
- Prototyping area
- 4 Indicators and 4 User's buttons
- Board has built in 5 volt regulator
- Power supplied to the board by way of a 2 position terminal block
- Power on LED
- Operating temperature 0 to 70C, extended temp available
- Machine screw sockets under all through-hole
- Two-layer 3.5" x 5" board
- Four corner mounting holes

1.3 Software Overview

The Rita-51J comes with four free software packages.

1.3.1 Reads51

[Reads51](#) is an Integrated Development Environment (IDE) to write application programs for the Rita-51 boards. It contains a C compiler, an assembler, a linker and a chip simulator. Any third party software development tools may be used for the Rita-51J. Reads51 comes free with Rigel's MCS-51 hardware products. Refer to the Reads51 User's Manual for more information.

1.3.2 Rita-51 Utility Software

The Rita-51 Utility Software from Rigel Corporation is a Windows program. It is an alternate means from the Reads51 software, to manage the on-board FLASH.

1.3.3 RitaBrowser

The [RitaBrowser](#) is a simple Windows socket (winsock) application to send and receive UDP messages. RitaHost maintains a list of RITA nodes (e.g., Rita-51 boards). You may connect to the boards and communicate with them by typing in the edit window. Refer to the RitaBrowser manual for more information.

1.3.4 Example Software

There are many example projects given with the Reads51 IDE that introduce the user to typical industrial applications of microcontrollers. These applications include timers, counters, serial communications, interrupt programming, analog-to-digital conversion, digital-to-analog conversion, stepper motors, LCDs, keypads, etc. A detailed exposure to microcontroller programming and applications may be found in textbooks published by Rigel Press (see www.rigelcorp.com/rigelpress.htm).

In addition, preliminary code is provided to experiment with the networking capabilities of the Rita-51J board. Most importantly, a library of network support functions, NetApi51, is provided. NetApi51 functions allow the user to quickly develop network applications for the Rita-51J in C or assembly. The NetApi51 functions currently support a subset of the standard TCP/IP stack, namely, ARP, ICMP, IP and UDP. This subset is sufficient to program the Rita-51J as an Internet (or a private intranet) node, which communicates through UDP messages.

Users are encouraged to modify the circuit diagrams and example software in developing their own specific applications. The source code of the user-accessible systems calls, as well as all examples on the distribution disk may be used or incorporated into applications by the registered buyer without any royalties, fees, or limitations. Rigel Corporation is not responsible for the suitability or correctness of the example software. Refer to warranty for additional information.

1.4 Package List

Your Rita-51J / READS package includes the following:
Rita-51J populated with 128K RAM, 128K FLASH PROM
Software, data sheets, and user's guide are downloadable from the web.
RJ-45 Cable supplied

A serial modem cable with a male DB9 connector and a 9 volt 500mA wall transformer are to be supplied by the user.

2 OPERATING MODES

2.1 Memory Architecture and Operating Mode

The memory architecture and the operating modes are determined by a complex programmable logic device (CPLD). Many different implementations are possible. Most OEM users have their own modes programmed into the CPLD at the factory. The CPLD programs may be modified in the field, provided that the user has access to a Xilinx 9500-series JTAG programmer. Contact Rigel Corporation for further information about custom operating modes. The following modes refer to the COTS (commercial off-the-shelf) version of the Rita-51J board.

The memory architecture refers to the manner in which memory is used. There are three architectures supported:

RIM (Rigel Industrial Module) architecture

RRM (Ram Resident Monitor) architecture

RROS (Rom Resident Operating System) architecture

The Reads51 IDE, allowing code to be placed in RAM or FLASH, supports these architectures. The memory architecture is determined by the jumper settings.

Each of these architectures supports two operating modes: the PRG (program) mode and the RUN mode. The mode is determined by the position of the slide switch. When switching between modes, move the slide switch and press the RESET push button. Note that the mode is toggled when the RESET pushbutton is pressed, not when the slide switch is moved. More specifically, the CPLD samples the state of the slide switch when a RESET event occurs. Two LEDs indicate the current mode. Use the PRG mode to erase and program the FLASH ROM. Once the FLASH is programmed with the application code, switch to the RUN mode.

Note that the default architectures use up to 64K of code memory and 64K of external data memory. Other custom architectures may be implemented to use more memory. Contact Rigel Corporation if you have a special need for a custom architecture. Bank switching must be used if all 128K of ROM and 128K of RAM are to be used. Almost all professional software tools support native bank switching capabilities. The Reads51 C compiler does not support bank switching. Most application require less than 64K of code or data memory.

The following table summarizes the jumper settings for the different architectures.

	RIM	RRM	RROS																																																						
First Jumper (Top position)	Removed	Left position	Left position																																																						
Second Jumper	Removed	Removed	Left position																																																						
Third Jumper	(Not used)																																																								
Fourth Jumper (Bottom position)																																																									
	<table border="1"> <thead> <tr> <th colspan="2">J5</th> <th>J4</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>AUX 0</td> <td>P 1.5</td> </tr> <tr> <td>GND</td> <td>AUX 1</td> <td>P 1.6</td> </tr> <tr> <td>GND</td> <td>AUX 2</td> <td>P 1.7</td> </tr> <tr> <td>GND</td> <td>AUX 3</td> <td>P 3.5</td> </tr> <tr> <td>GND</td> <td>AUX 4</td> <td></td> </tr> </tbody> </table>	J5		J4	GND	AUX 0	P 1.5	GND	AUX 1	P 1.6	GND	AUX 2	P 1.7	GND	AUX 3	P 3.5	GND	AUX 4		<table border="1"> <thead> <tr> <th colspan="2">J5</th> <th>J4</th> </tr> </thead> <tbody> <tr> <td colspan="2" style="background-color: black;"></td> <td>P 1.5</td> </tr> <tr> <td>GND</td> <td>AUX 1</td> <td>P 1.6</td> </tr> <tr> <td>GND</td> <td>AUX 2</td> <td>P 1.7</td> </tr> <tr> <td>GND</td> <td>AUX 3</td> <td>P 3.5</td> </tr> <tr> <td>GND</td> <td>AUX 4</td> <td></td> </tr> </tbody> </table>	J5		J4			P 1.5	GND	AUX 1	P 1.6	GND	AUX 2	P 1.7	GND	AUX 3	P 3.5	GND	AUX 4		<table border="1"> <thead> <tr> <th colspan="2">J5</th> <th>J4</th> </tr> </thead> <tbody> <tr> <td colspan="2" style="background-color: black;"></td> <td>P 1.5</td> </tr> <tr> <td colspan="2" style="background-color: black;"></td> <td>P 1.6</td> </tr> <tr> <td>GND</td> <td>AUX 2</td> <td>P 1.7</td> </tr> <tr> <td>GND</td> <td>AUX 3</td> <td>P 3.5</td> </tr> <tr> <td>GND</td> <td>AUX 4</td> <td></td> </tr> </tbody> </table>	J5		J4			P 1.5			P 1.6	GND	AUX 2	P 1.7	GND	AUX 3	P 3.5	GND	AUX 4	
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In general, the RRM architecture is convenient for downloading and testing programs. Since code is downloaded into RAM, there is no need to erase the FLASH ROM. However, if power is lost during operation, the code in RAM will be lost.

The RIM architecture uses no jumpers. It is intended for the case where Rita-51J is used in the embedded controller. Since code is in FLASH ROM, code is not lost when the board is disconnected from power. However, the RIM architecture may be a little inconvenient for debugging, since the FLASH ROM has to be erased before a new program may be downloaded.

The RROS architecture is intended for the case where the Reads51 assembly-level debugging is to be used.

Note that, in the basic COTS versions of Rita-51J, code memory and data memory do not overlap in the RIM architecture. Contact Rigel Corporation if you would like to implement other configurations.

In the RIM and RRM modes, if the Rita-51J is used with a third-party software debugger, the monitor must be downloaded along with the program. This arrangement is convenient in supporting a wide range of third-party software development tools.

2.1.1 The RIM Architecture

The RIM architecture is selected when there are no jumpers inserted into J5. The RIM architecture uses 64K of FLASH ROM memory for code and 64K of RAM for XDATA memory. In the PGM mode the RIM monitor allows erasing FLASH ROM and loads the user code.

Connect the Rita-51J to the serial port and run the Reads51 TTY window. Select a suitable Baud rate. Move the slide switch to the PGM position and press RESET. Then tap on the space bar a few times. The RIM monitor prompt appears.

You may erase the FLASH ROM by typing 'e' (case sensitive). Once the FLASH ROM is erased, download your code into ROM by using the Reads51 Compile / Download Hex File menu command.

Note that the RIM monitor extracts the Baud rate from the space characters received. You may need to press the space bar a few times. Also note that not all Baud rates are possible with a given oscillator frequency. Download the utility Baud.exe from the Rigel website to see which Baud rates are possible with a given oscillator frequency.

Once the code is downloaded to FLASH ROM, move the slide switch to its RUN position. Press the RESET button to execute the downloaded program. Note that the execution starts at address 0.

2.1.1 The RRM Architecture

The RRM architecture is similar to the RIM architecture. However, both CODE and XDATA memory blocks are mapped into the RAM, while the FLASH is not used. The 128K RAM is partitioned into 64K of CODE memory and 64K of XDATA memory. The RRM architecture is selected when there is a jumper placed in the top left position of J5.

Connect the Rita-51J to the serial port and run the Reads51 TTY window. Select a suitable Baud rate. Move the slide switch to the PGM position and press RESET. Then tap on the space bar a few times. The RRM monitor prompt appears.

Since FLASH ROM is not used, you may download your code into RAM by using the Reads51 Compile / Download Hex File menu command.

Note that the RRM monitor extracts the Baud rate from the space characters received. You may need to press the space bar a few times. Also note that not all Baud rates are possible with a given oscillator frequency. Download the utility Baud.exe from the Rigel website to see which Baud rates are possible with a given oscillator frequency.

Once the code is downloaded to RAM, move the slide switch to its RUN position. Press the RESET button to execute the downloaded program. Note that the execution starts at address 0.

2.1.3 The RROS Architecture

The RROS architecture support is maintained for those who want to use the assembly language debugging features of the monitor. RROS is backwardly compatible with the earlier version of Reads51 (even version 1 of 1989). The RROS architecture requires an 11.0592 MHz clock oscillator. It uses 32K of ROM monitor and 32K of RAM for a total of 64K of memory. The CODE and XDATA memory spaces are overlapped.

In the PRG mode, the ROM monitor occupies the lower half of memory, and RAM, the upper half. In the RUN mode, the RAM occupies the lower half, and the ROM monitor, the upper half. This allows downloading programs into RAM and running them starting from address 0. Of course, programs may be run while keeping RAM in the upper half of memory (address 8000h to FFFFh). The start address of the Reads51 debugger directs the program execution to the start of the user program.

Connect the Rita-51J to the serial port and run the Reads51 TTY window. Make sure that an 11.0592 MHz clock oscillator is used. Select 9600 Baud. Move the slide switch to the PGM position and press RESET. The RROS monitor will appear.

You may download your code into RAM by using the Reads51 Compile / Download Hex File menu command, or by switching to the Reads51 Run/Debug mode.

2.2 Interfacing the Rita-51J

The Rita-51J has connections to Port 1 and 4 bits of Port 3. Each port may be used as either an input or an output port. The 8051 ports may be operated in the 8051 mode. That is, the ports contain open-drain transistors with pull-up resistors. In this mode, when used as output ports, it is recommended that the ports sink current. Similarly, when used as input ports, first write 1's to the ports and have the external signal drive the port low. External Memory-mapped I/O may be attached to the Rita-51J. All address, data and control signals for such interfacing are available on header J10.

3 OPERATING NOTES

3.1 Overview

Rita-51J uses the 8051 family of microcontrollers in the standard 44-pin PLCC package. These microcontrollers use the MCS-51 instruction set. The Rita-51J uses external RAM during the development cycle. Once an application program is developed, it may be permanently placed in FLASH. With an application-specific program installed, the Rita-51J may be used as an embedded controller.

The considerable flexibility of the Rita-51J is achieved by placing various monitor and loader programs in both internal code memory of the microcontroller and in the first segment of FLASH ROM. If you would like to run the Rita-51J with a different microcontroller, contact Rigel corporation to obtain a chip with these programs already installed in internal code memory.

The following are general guides to operating the board.

3.2 J6 Power Input

Power is brought to the Rita-51J board by a two-position screw-type terminal block, J6. The Rita-51J has a 5 volt regulator built in so you may use a 9-12 volt AC or DC wall transformer for power. We recommend a 9 volt, 500 mA transformer.

3.3 Serial Ports, P1 and P2

The CPU serial port on the Rita-51J is accessed through an RS-232 level converter in U8. The microcontroller supports transmit and receive signals. P1 of the Rita-51J is a DB-9 female connector used to connect the board to an IBM compatible PC. A minimal serial port is constructed with just 3 lines: transmit, receive, and ground, disregarding all hardware handshake signals. A straight-through modem cable should be used. That is a cable connecting pin 2 of the Rita-51J to pin 2 of the host, and similarly pin 3 to pin 3, and pin 5 to pin 5.

The second serial port P2, on the Rita-51J is optional and only available when using the DS87C520 or a similar 8051, which supports 2 serial ports. The DB-9 connector P2 may be used to communicate with the PC host during programming and debugging the board.

If the second serial port is used, insert jumpers J1 (RxD1) and J2 (TxD1). These jumpers connect the ports P1.2 and P1.3 to the RS-232 level converter U8. In this case, ports P1.2 and P1.3 are dedicated to the second serial port, and should not be used as general-purpose I/O.

3.4 J3 The Ethernet Port

Socket J3 accepts 10Base-T signals terminating at an RJ-45 connector. J3 is Rita-51J's primary means to connect to a 10Mbit Ethernet network. Note that J3 also includes the magnetics (transformers) needed to electrically isolate the Ethernet signals from the LAN.

3.5 Push Buttons

The Rita-51J has one reset button and four user buttons. The reset button PB1 resets the board. The four user buttons may be connected to external circuitry via header J7. Typically these buttons would be attached to the microcontroller ports and used to debug your software.

3.6 Slide Switches

The slide switch S1 located between the LEDs changes the operating mode of the board. When the slide switch is in the Program (PGM) mode you may download software to the FLASH ROM. The RUN position allows you to run your program from ROM. The precise effect of the slide switch depends on the memory configuration (referred to as the memory mode, or simply as the mode) selected by the jumpers.

The second slide switch S2 located above the pushbutton is the power switch. Slide S2 to the "ON" position to run the board.

3.7 LEDs

There are six LEDs on the Rita-51J. Two of the LEDs indicate the current operating mode of the board. The other four LEDs may be connected to external circuitry via header U8.

3.7.1 Status LEDs

The two LEDs next to the slide switch are used as status indicators. The LEDs light up depending on the operating mode, which in turn is determined by the position of the slide switch. The red LED is on while the board is in the Program (PGM) mode. It is turned off when the board enters the RUN mode. The green LED turns on when the board is in the RUN mode.

3.7.2 User LEDs

There are four LEDs by the prototyping area, which are designated as User LEDs. They may be connected to external circuitry by way of header J8. Typically these buttons would be attached to the microcontroller ports and used as I/O for the application, or perhaps, used to debug your software.

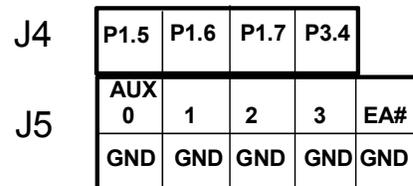
3.8 Headers

The Rita-51J board has ten headers, as summarized below.

Header	Name	Function
J1	RxD1	Connects second serial port receive signal to P1.2
J2	TxD1	Connects P1.3 to the second serial port transmit signal
J4	Options	Connects microcontroller ports P1.5, P1.6, P1.7, and P3.4 to the CPLD inputs. Not used in the COTS version.
J5	Options	CPLD options inputs.
J7	UI	User inputs (pushbuttons)
J8	UO	User outputs (LEDs)
J9	Ports	Microcontroller ports for interfacing
J10	System	System signals (address, data, and control signals) for external hardware interfacing.
J11	VCC	Regulated 5 V supply for user circuitry
J12	GND	Regulated power supply ground for user circuitry

3.8.1 J4 and J5

The Rita-51J uses a complex programmable logic device (CPLD) to determine the operating modes, memory map. Many different implementations are possible. J4 and J5 are the options headers for the CPLD. J5 is a 2-by-5 header. The last position, marked EA# is not used in the COTS models. Inserting a jumper in these positions selects among the various architectures. Insert a jumper in the top position (0) to select the RRM mode. Insert jumpers in both the top and the next position (0 and 1) to select the RROS architecture.



J4 is available if some of these signals are to be automatically provided by the microcontroller ports. In the COTS version, the signals on J4 are not used so that all ports are available for user I/O.

3.8.2 J7 and J8

Headers J7 and J8 are for the four user push buttons and LEDs. The push buttons and LEDs are typically connected to the I/O ports or external circuitry built on the prototyping area.

3.8.3 J9 I/O Header

The I/O header is a two-row 20-pin header. The I/O header contains Port 1, and Port 3.2 to 3.5, an active-low reset input, GND, VCC, and the transmit and receive signals for the serial ports. Note that two serial ports are available only when the

Rita-51J is populated with the DS87C520 or DS89C420 microcontroller. In this case, ports P1.2 and P1.3 are dedicated to the second serial port, and should not be accessed on J9. Individual signals of these jumpers are listed below. Pin 1 may be identified as the post with the square pad on the printed circuit board.

Pin	Signal	Pin	Signal
1	VCC	2	P3.2
3	P1.0	4	P3.3
5	P1.1	6	P3.4
7	P1.2	8	P3.5
9	P1.3	10	EEP
11	P1.4	12	TXD0
13	P1.5	14	RXD0
15	P1.6	16	TXD1
17	P1.7	18	RXD1
19	RSTIN#	20	GND

Notes:

1. The second serial port is available when the board is populated with the DS87C520 microcontroller.
2. Do not use P1.2 and P1.3 if the board is populated with a DS87C520 or DS89C420 microcontroller with two serial ports.
3. Pins 16 and 18 are available only if the board is populated with a DS87C520 or DS89C420 microcontroller.
4. RSTIN# is an active-low input signal. It is inverted and used as a reset input to the microcontroller and to the Ethernet driver.
5. EEP is connected to the data pin of a DS2502E48 memory device with a unique MAC (Ethernet) address.

3.8.4 J10 System Header

The system bus is available on a two-row 40-pin header marked J10. The pin assignments are given below. The address and data lines of the microcontroller are de-multiplexed. The system bus facilitates interfacing the Rita-51J to external memory-mapped input/output devices.

Pin	Signal	Pin	Signal
1	VCC	2	(not used)
3	A0	4	D0
5	A1	6	D1
7	A2	8	D2
9	A3	10	D3
11	A4	12	D4
13	A5	14	D5
15	A6	16	D6
17	A7	18	D7
19	A8	20	(not used)
21	A9	22	RSTIN#
23	A10	24	RSTOUT#
25	A11	26	RSTOUT
27	A12	28	XIOSEL#
29	A13	30	RAMRD#
31	A14	32	RAMWR#
33	A15	34	(not used)
35	A16	36	(not used)
37	A17	38	(not used)
39	A18	40	GND

4 SOFTWARE

4.1 System Requirements

All of Rigel's software products are designed to work with an IBM PC or compatible, Pentium 120MHz or better, running Windows 95, 98, NT, 2000, PE, or XP. The newest version of the software is always available to download off our web site, www.rigelcorp.com. We encourage you to check our web site often to keep up-to-date.

4.2 Software Installation

If you receive a CD from Rigel, follow these steps:

Place the CD-ROM in your drive. Go to the **Rigel Products \ 8051Software \ Reads51 \ Win95-nt** and click on the software file you wish to install. The program will then install in your system.

Follow the standard install directions.

If you download the software from www.rigelcorp.com, click on the .exe file. The program will then install in your system. Follow the standard install directions.

4.3 Reads51

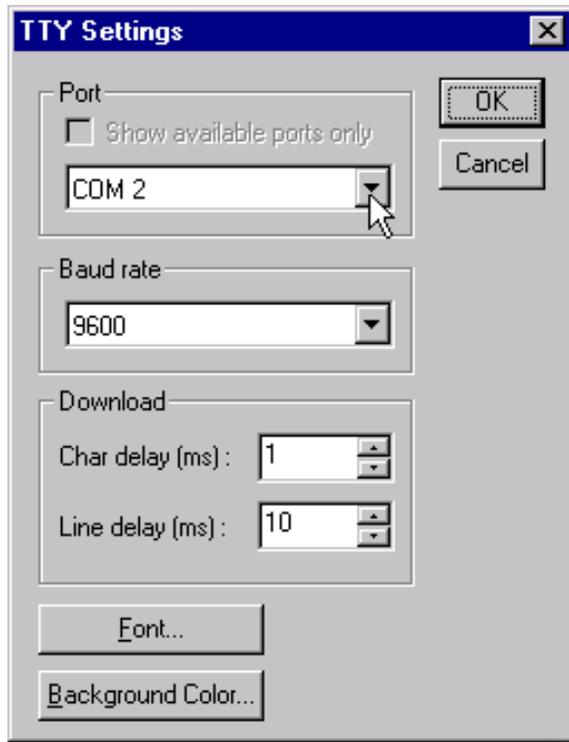
Reads51 is an Integrated Development Environment (IDE) used to write application programs for the Rita-51J boards. It contains a C compiler, an assembler, a linker and a chip simulator. Any third party software development tools may be used for the Rita-51J. The following sections are designed to help get you started with the Reads51 and Rita-51J. For detailed information about the Reads51 software refer to the Reads51 User's Manual.

4.3.1 Rita-51J Start-Up With Reads51

Check to make sure the slide switch is in the MON position.

Connect Rita-51J to the PC host via a modem cable.

Connect Rita-51J to a power supply. The red LED should light up when power is connected.



Run the Reads51 IDE by selecting **Start | Programs | Reads51**. You may also start Reads51 by double clicking on the Reads51 short cut icon if installed. Specify the serial port (COMM Port) that is connected to the board by opening the Options | TTY Options window.

Select the Toolchain and Target platform by selecting Options | Toolchain/Target and selecting Reads51 Toolchain v4 and the target RR0S.

Open the TTY window using the menu command View | TTY Window.

Press RESET on the embedded controller board and hit the space bar on the computer you are using, observe the prompt in the TTY window.

4.3.2 Verifying that the Monitor is Loaded

Make sure the TTY window is active, clicking the mouse inside the TTY window to activate it if necessary. Then type the letter '**H**' (case insensitive) to verify that the monitor program is responding. The '**H**' command displays the available single-letter commands the monitor will recognize.

The READS monitors use single-letter commands to execute basic functions. Port configurations as well as memory inspection and modifications may be accomplished by the monitor. Most of the single-letter commands are followed by 4 hexadecimal digit addresses or 2 hexadecimal digit data bytes.

The list of monitor commands is displayed with the **H** command while the monitor program is in effect. The **H** command displays the following table.

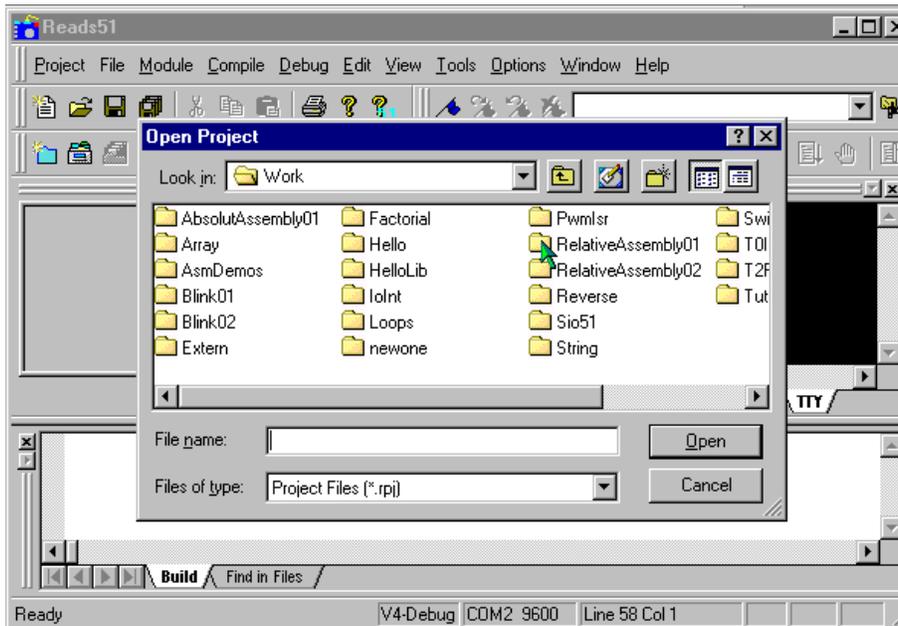
B xxxx	sets Break point at address xxxx
C xxxx-xxxx	displays Code memory
D xx-xx	displays internal Data ram
D xx=nn	modifies internal Data ram
D xx-xx=nn	fills a block of internal Data ram
G xxxx	Go - starts executing at address xxxx
H	Help - displays monitor commands
K	Kills (removes) break point
L	down Loads Intel hex file into memory
Px	displays data on Port x
Px=nn	modifies data on Port x to nn
R	displays the contents of the Registers
S	displays Special function register addresses
S xx-xx	displays Special function registers
S xx=nn	modifies Special function registers
S xx-xx=nn	fills Special function registers
X xxxx-xxxx	displays eXternal memory
X xxxx=nn	modifies eXternal memory
X xxxx-xxxx=nn	fills eXternal memory

A single-letter command may be followed by up to 3 parameters. The parameters must be entered as hexadecimal numbers. Each 'x' above represents a hexadecimal digit (characters 0..9, A..F). Intermediate spaces are ignored. Alphabetic characters are converted to upper case. The length of the command string must be 16 characters or less. The command syntax is:

Letter [address][-address][=data]<CR>.

4.3.3 Downloading and Running an Assembly Program

Use the use the **Project | Open Project** command to open the project



"AbsoluteAssembly01".

Assemble the program using the **Compile | Build** command.

Use the **Compile | Toggle Mode** command to switch to the Run/Debug Mode.

Click on the **Compile | Run** command and specify the starting address 8000 (hex).

Again the **Compile | Toggle Mode** command to revert back to the Build Mode.

4.3.4 Downloading and Running a C Program

Use the **Project | Open Project** command to open the project "Hello".

Compile the program and download it to the board using the **Compile | Build and Download** command. The project will be compiled and the resultant HEX code will be downloaded to the target board.

Press and hold the RESET button on the board. While the RESET button is pressed, flip the MON / RUN switch to the RUN position. This swaps the memory map on the board so that RAM occupies low memory. The HEX code downloaded to RAM executes when you release the RESET button.

4.3.4 Programming On-Board FLASH with Reads51

Reads51 may be used to manage the on-board FLASH of the Rita-51J. In the Options | Toolchain/Target dialog, select either the RR0S or the RRM target. Also select an available port and a suitable Baud rate (i.e. 9600) in the Options | TTY Options dialog. Open the TTY window. Make sure that the Rita-51J is in the PGM mode (slide switch towards the red LED). Press RESET and then hit the space bar. The Baud rate is detected and used by the Rita-51J.

In order to erase the FLASH, simply type the letter 'e' (case sensitive). Once erased, the FLASH may be programmed. Use the Compile | Download HEX... menu to select a HEX file. The download progress is reported in the status bar.

4.4 Rita-51 Utility Software

The Rita-51 Utility Software from Rigel Corporation is a Windows program. It is an alternate means, from the Reads51 software, to manage the on-board FLASH.

Select the COMM port and a Baud rate. The Rita-51 Utility detects the Baud rate from the board. The set of acceptable Baud rates depends on the crystal



frequency. Typically, 9600 works with all frequencies. The standard 11.0592 MHz frequency often used with 8051 microcontroller allow almost all Baud rates up to 57600. With a 24 MHz crystal, the highest Baud rate is 11520. Higher frequencies do not necessarily allow higher Baud rates. The crystal frequency must be an even multiple of the Baud rate, or at least within a few percent of the ideal value. Move the slide switch on the Rita-51J to the PGM (program) position, press the reset push button and press the space bar to see the Rita-51 monitor prompt.

The Rita-51 Utility has two buttons. The "Erase" button erases the FLASH ROM. The "Download" button asks for a program file in the Intel hex format. It opens and downloads the file to the board. Once you download your program, move the slide switch to the RUN position and press the reset push button. Your code in FLASH ROM now constitutes the 8051 code memory. The RAM is mapped into the 8051 external data (XDATA) memory.

4.5 RitaBrowser

RitaBrowser monitors and controls Internet appliances built with Rigel Corporation's Rita family of control boards. The Rita nodes may be on the Internet or on a private network such as a personal network or a company intranet.

4.5.1 Configuring RitaBrowser

Click the "Configure" button. Use the tab "This PC" to specify the IP address of your computer. If you are using a dial-up service, you can obtain the IP address by the "ARP" utility. Open a DOS box and type "arp -a" to see your assigned IP address. If your PC is set to participate in a LAN, use the "Settings / Control Panel /Network" dialog to view your IP address.

If you would like to automatically launch programs on your PC when a keyword is



received from a Rita node, enter the (case sensitive) keyword and select the program to be activated. Note that the parameters received from the Rita node following the keyword are passed on to the launched program as command line parameters.

The "Ping timeout" is currently not used. The "Port" address determines the UDP part your PC uses to communicate with the Rita node. Unless you are using this value in the Rita program, you may click the "Auto" box.

The "Rita Nodes" tab in the configuration dialog lists the current nodes. You may add, modify, or remove nodes from the list. When adding new nodes, you will be asked to provide a name along with the IP address and port number for the Rita

node. The name is used by the RitaBrowser to identify the node. This is like a "bookmark" or a "favorite" entry in a web browser. The default Rita port number is 8192 (0x2000). You may change this number, especially if you intend to use it to identify among various services at the Rita node.

Advanced Configuration

You may save the list of Rita nodes to a file as a backup or to load onto another PC. When loading a Rita nodes list, you will be asked if you would like to append the new list to the existing one or to replace the existing list with the new list. In the former case, you will also be notified if there are duplications or conflicts.

4.5.2 Communicating With a Rita Node

A list of currently known Rita nodes appears in a drop-down list box. Select the node you would like to communicate with and click the "Connect" button. RitaBrowser opens a socket to communicate with the Rita node. If the socket cannot be opened, it usually means that you have not correctly specified your PC's IP address. Once a socket is successfully opened, you may type in the edit window and communicate with the Rita node. Note that the communication depends on the specific program running on the Rita node. Being an open architecture, you are free to program the Rita node any way you wish. For instance, you may use restrict the node to answer only to specific IP addresses, or use the port numbers to invoke different behaviors. Refer to the Rita hardware and programming manuals for further information and demo programs. It is recommended that a Rita node responds with a short message, possibly a menu, when it receives an unknown command or the question mark ('?').

5 CPLD EQUATIONS

The CPLD equations are given in ABEL (advanced Boolean expression language).

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```
module RITAJ5V1
Title 'RITAJ_U5'

RITAJ_U5 device;

WRX      pin 2 istype 'com, input';
RDX      pin 3 istype 'com, input';
PSENX    pin 4 istype 'com, input';

A8        pin 5 istype 'com, input';
A9        pin 6 istype 'com, input';
A10       pin 7 istype 'com, input';
A11       pin 8 istype 'com, input';
A12       pin 9 istype 'com, input';
A13       pin 11 istype 'com, input';
A14       pin 12 istype 'com, input';
A15       pin 13 istype 'com, input';

RIMMODE   pin 14 istype 'com, input';
RRMMODE   pin 18 istype 'com, input';
AUX2      pin 19 istype 'com, input';
PA16X     pin 20 istype 'com, input';

EAX       pin 22 istype 'com, input';
PRG       pin 24 istype 'com, input';
RSTX      pin 40 istype 'com, input';

// --- outputs ---
ROMSELX   pin 1 istype 'com, output';
RAMSELX   pin 44 istype 'com, output';
MRDX      pin 43 istype 'com, output';
MWRX      pin 42 istype 'com, output';

RSTOUT    pin 39 istype 'com, output';
RSTOUTX   pin 38 istype 'com, output';

RSTNET    pin 37 istype 'com, buffer';
NETSELX   pin 36 istype 'com, buffer';

XIOSELX   pin 35 istype 'com, buffer';
XSEL_1X   pin 34 istype 'com, buffer';
XSEL_2X   pin 33 istype 'com, buffer';
XSEL_3X   pin 25 istype 'com, buffer';
```

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```
MA15      pin 26 istype 'com, buffer';
MA16      pin 27 istype 'com, buffer';

LEDMONX   pin 28 istype 'com, buffer';
LEDRUNX   pin 29 istype 'com, buffer';

// --- unused pins (must be unused for the logic to fit) ---
// tie to GND or VCC: 3, 4, 5, 6, 25, 39

// --- nodes ---
PRGMODE node istype 'reg, buffer';

"
" RIMMODE (AUX0) and RRMMODE (AUX1) determine the memory map
" ROM (FLASH) high segment holds the RROS monitor
"-----
" remove jumper (RIMMODE=1) to download code to FLASH.
"
"           code memory           data memory
"           -----
"
" PRGMODE=1 : internal           ROM (low segment)
" PRGMODE=0 : internal+ROM       RAM (low segment)
"-----
" insert jumper (RIMMODE) for the RROS or RRM mode.
" with RRMMODE removed, RAM holds both CODE and XDATA.
"
"           code memory           data memory
"           -----
"
" PRGMODE=1 : ROM (high segment)  RAM (low segment)
" PRGMODE=0 : RAM (low segment)   RAM (high segment)
"-----

equations

PRGMODE    := !PRG;
PRGMODE.ck = !RSTX;

LEDMONX = !PRGMODE;
LEDRUNX = PRGMODE;

RSTOUT = !RSTX;
RSTOUTX = RSTX;
```

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```
RSTNET = !RSTX;

// use AUX2 so that the cpld compiler does not fuss
XSEL_1X = RRMODE;
XSEL_2X = AUX2;
XSEL_3X = PA16X;

when PRGMODE then
{
  MWRX = WRX;
  XIOSELX = 1;
  NETSELX = 1;

  when (RIMMODE) then
  {
    MRDX = RDX;
    EAX = 1; // monitor in internal code memory
    MA15 = A15;
    MA16 = !PA16X; // allow programming segment 1
//    MA16 = 0;
    ROMSELX = 0; // program FLASH ROM
    RAMSELX = 1;
  }
  else
  {
    EAX = 0; // monitor in FLASH ROM high segment

    MA15 = A15;

    MRDX = RDX & PSENX;

    when (RRMMODE) then
    {
      MA16 = !PSENX; // activate monitor when reading code memory
      ROMSELX = PSENX;
      RAMSELX = RDX & WRX;
    }
    else // RROS mode
    {
      MA16 = !A15; // FLASH high seg when ROMSELX
      ROMSELX = A15;
      RAMSELX = !A15;
    }
  }
}
```

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```
    }
    else // RUNMODE
    {
        EAX      = 0; // all code is external

// [FD00..FDFF]
    NETSELX = !(PSENX & A15 & A14 & A13 & A12 & A11 & A10 & !A9 & A8); // [FD00..FDFF]
// NETSELX=1;

// [FE00..FEFF]
    XIOSELX = !(PSENX & A15 & A14 & A13 & A12 & A11 & A10 & A9 & !A8); // [FE00..FEFF]

    when (RIMMODE) then
    {
        MA15    = A15;
        MA16    = 0; // use only low segments
        ROMSELX = PSENX; // program FLASH ROM
        RAMSELX = (RDX & WRX) # !XIOSELX # !NETSELX;
        MRDX    = RDX & PSENX;
        MWRX    = WRX;
    }
    else
    {
        MRDX    = RDX & PSENX;
        MWRX    = WRX;

        when (RRMMODE) then
        {
//      RAMSELX = 0; // code in RAM low segment
            RAMSELX = PSENX & !(XIOSELX & NETSELX);
            ROMSELX = 1;
            MA15    = A15;
            MA16    = PSENX; // code in low segment
        }
        else
        {
// lower 32K of overlapped CODE/XDATA in FLASH
// similar to the PRGMODE, but with 32K banks swapped

//ROMSELX = !A15;
            ROMSELX = !A15 # !(XIOSELX & NETSELX);
            RAMSELX = A15;

            MA15    = !A15; // swap 32K banks
        }
    }
}
```

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```
        MA16 = A15; // FLASH high seg when ROMSELX
    }
}
end RITAJ5V1
```

6 BILL OF MATERIALS

The bill of materials given below lists all components by their reference as they appear on the board top overlay.

Revised: July 2003

List Of Materials

Item	Quantity	Part	Reference
	QUANTITY	PART	DESIGNATOR
1	1	560pF	C3
2	20	10nF	BP, 4, 5, 7, 9
3	2	100nF	C1, C2
4	4	1uF	C10-13
5	3	47uF	C8, 31, 32
6	1	220uF	C6
7	2	8 Ohm	R2, R3
8	1	100 Ohm	R5
9	1	4.7K	R6
10	1	4.99K	R7
11	1	680 Ohm 10Gang	R4
12	2	10K Gang	R1, R8
13	1	Varisater	V1
14	5	Red LEDs	D1, D4-D7
15	1	Green LED	D2
16	1	Bridge	D3
17	5	Push Button	PB1-PB5
18	2	Slide Switch	S1, S2
19	2	DB9's	P1, P2
20	1	3.5mm Terminal Block	J6
21	1	Belfuse RJ45	J3
25	2	1X2 Header	J1, J2
26	1	1X3 Header	J11, J12
27	3	1X4 Header	J4, J7, J8
28	2	2x5 Header	J5
29	1	2x10 Header	J9
30	1	2x20 Header	J10

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31	1	20MHz	X2
32	1	24MHz / 32MHz	X1
33	1	89C52	U1
34	1	CS8900A-CQ	U4
35	1	MAX232	U8
36	1	74HCT573	U2
37	1	AM29F010	U3
38	1	XC9536-	U5
39	1	DS1233	U6
40	1	62128	U7
41	1	7805	U9
42	1	DS2502-E48	U10

8. CIRCUIT DIAGRAM

9 REFERENCES

Rita-51 User's Guide, Rigel Corporation, www.rigelcorp.com, 2002.

CS8900A Product Data Sheet, Cirrus Logic, www.cirrus.com, 2001, (cs8900a-4.pdf).

Using the Crystal 8900A in 8-Bit Mode, by James Ayres, Application Note AN181, www.cirrus.com, 2000, (an181.pdf).

CS8900A Frequently Asked Questions, Application Note AN205, www.cirrus.com, 2001, (an205-1.pdf).

Crystal LAN CS8900A Ethernet Controller Technical Reference Manual, by Deva Bodas, revised by James Ayres, Application Note AN83, www.cirrus.com, 2001, (an83-3.pdf).

Appendix

A. USING THE RITA-51J BOARD

This appendix is subject to change at any time. For the latest information, software, and examples please check our website often.

A.1 Overview

The Rita51 board has all the necessary hardware to connect the 8051 microcontroller to an Ethernet network. With appropriate software, the board may be used as an Internet node (host). A complete TCP/IP implementation is beyond the scope of this document. The range of capabilities depends on the limited memory and processing power of the 8-bit microcontroller. However, many TCP/IP applications are possible. Note that there are several professional TCP/IP software vendors who support the 8051 architecture. (Refer to the website www.rigelcorp.com for links.)

This document presents a few projects that may be used to verify the functionality of the Rita51 and its Ethernet connection. Please note that the software is currently under development. Many of the lower-level functions are written in assembly and collected into the two libraries. The low-level source code is subject to change, and is thus not yet released.

A.2 EXPERIMENTS

You may conduct several experiments with the Rita51. These experiments assume that you connect the Rita51 to a network, and that your PC is connected to the same network. Note that your PC should also be connected to the Rita51 through a serial port. This connection is used to download the programs into the Rita51. It is also used in the experiments for the Rita51 to report its activity.

If your PC is not on a network, you may simply connect the Rita51 to the PC's Ethernet port with a crossover cable. The two devices (the PC and the Rita51) become the two (and only two) nodes on the network.

If you use an existing network, you need an IP (internet protocol) number for the Rita51. Select this number so that it does not conflict with other hosts on the network.

The experiments assume the IP address of the Rita51 board to be 192.168.0.64. You may change this by modifying the source and recompiling the project. Similarly, the board is assigned the ether MAC (media access control) address 5.4.3.2.1.0. Again, this may be changed in the source and recompiled.

A.2.1 Sniff Experiments

Once the PC and the Rita51 is connected to the network, you may conduct several experiments. The two projects Sniff_Ether and Sniff_IP run the Rita51 as a "sniffer." Here the Rita51 listens to the message traffic on the network and

reports the messages out its serial port. Your PC's serial port connection receives these reports.

A.2.2 Ping Experiment

The two experiments Sniff_Ether and Sniff_IP call the function NetServiceMsgs() to process the incoming messages. A more detailed description of this function is given in Section 3.2 below. Sniff_Ether() passes the argument FALSE (zero) to NetServiceMsgs(). Sniff_IP, on the other hand, passes a nonzero argument (TRUE). This instructs NetServiceMsgs() to process ARP (address resolution protocol) and ICMP echo request/reply (ping) messages. Run Sniff_IP on the Rita51. Then, from a DOS box on the PC, issue the command

```
ping 192.168.0.64
```

This invokes the Windows ping application and sends a data packet, expecting it to be echoed back. The ping utility then reports the time it takes the echo to be received. Sniff_Ether does not process the echo request. IT may be used to inspect the messages received from the ping utility.

A.2.3 RitaPorts Experiment

The experiment RitaPorts runs over UDP (user datagram protocol). It communicates with the PC over the ethernet connection. You may use any software that is capable of sending and receiving UDP messages (such as netcat). The Windows application RitaBrowser is written specifically for this purpose. You may download RitaBrowser from the Rigel website www.rigelcorp.com. It is a simple "TTY-like" interface that sends the keystrokes out as UDP messages, and displays the UDP messages received in its window. With RitaBrowser, you may type in commands, which are sent over the ethernet connection from your PC through the network, and finally to the Rita51. The responses travel from the Rita51, through the network, and arrive at your PC. These responses are displayed in the window of the RitaBrowser. The simple application RitaPorts implements a menu that runs on the Rita51. The user may read the port values of the Rita51 over the network as well as set the port values.

A.3 PROGRAMMER'S VIEW

Rita51 network connectivity software is comprised of two libraries. NetStack51 contains the low level routines and hardware drivers. It also contains the code, written in low-level assembly, to perform ARP and ICMP echo requests.

NetApi51 contains the higher-level routines, which are called by the application. NetApi51 has two modules. Module "Network" uses C code. This is the module that may be customized for specific applications. Module "NetworkLow" contains lower level routines, many of which are written in in-line assembly.

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The application performs network communications by calls to NetApi51 routines. NetApi51 is UDP-oriented. That is, there are many functions in the library to support transmitting and receiving UDP messages.

The Rita51 family of boards uses the CA8900A network driver chip. The CS8900A does not support interrupts in the 8-bit mode. Thus, NetApi51 routines are polling oriented.

A.3.1 Network Initialization

```
void NetSetEtherAddress(unsigned int u2, unsigned int u1, unsigned int u0);
```

Sets the six-byte ethernet address, also known as the hardware address or the IEEE address. For example, `NetSetEtherAddress(0x0504, 0x0302, 0x0100);` sets the ethernet address to 0x050403020100. It is customary to separate the individual bytes of the address by hyphens and write them in decimal, as 5-4-3-2-1-0.

```
void NetSetIPAddress(unsigned int u1, unsigned int u0);
```

`NetSetIPAddress()` sets the four-byte logical internet protocol (IP) address. For example, `NetSetIPAddress(0xC864, 0x6402);` sets the IP address to 0xC8646402. It is customary to separate the individual bytes of the address by periods and write them in decimal. Here, 0xC0A80040 is written as "192.168.0.64".

```
int NetInitialize(int uMode);
```

`NetInitialize()` initializes the variables and the network driver chip. The network driver chip takes about 10 milliseconds after reset to complete its internal initialization. The function returns zero when initialization is completed. Otherwise, it returns a non-zero busy code. The argument determines the type of messages to be accepted. The following constants are defined:

<code>IM_PROMISCUOUS</code>	allows all messages
<code>IM_BROADCAST</code>	allows messages with broadcast ethernet address (e.g., FF-FF-FF-FF-FF-FF)
<code>IM_INDIVIDUAL</code>	allows messages with an ethernet destination address equal to the ethernet address of this node (set previously by a call to <code>NetSetEtherAddress()</code>).

Any combination of the constants may be specified by combining them with the logical "or" operation. Typically an application calls the initialization routine with its argument set to `(IM_BROADCAST | IM_INDIVIDUAL)`. Note that broadcast messages must be allowed for the node to respond to ARP messages. `IM_PROMISCUOUS` should be set to sniff all message traffic. However, this may overwhelm the node, missing some of the messages.

A.3.2 Message Reception

A few steps are involved in receiving messages. First the network driver is polled to see if a message is pending at the network driver chip. Pending messages are copied from the network driver chip to external RAM and processed. Flags in external RAM are used to specify the results of polling and of the state of reception. There are three primary flags: E_MSGRDY, IPIN_MSGRDY, and UDPIN_MSGRDY.

The function NetServiceMsgs() clears the UDPIN_MSGRDY flag and polls the network driver. E_MSGRDY is set if a raw (ethernet) message is pending (in the local memory of the network driver chip). NetServiceMsgs() takes a Boolean argument. If zero (FALSE), the function returns with the state of reception reflected in E_MSGRDY. If the argument is non-zero (TRUE), the function further processes the message. First, it is copied from the local memory of the network driver chip to external RAM. Then the two flags IPIN_MSGRDY and UDPIN_MSGRDY are cleared. The message is inspected. If the message is an ARP message (LLC=0806), it is automatically serviced. If the message is an IP message (LLC=0800) the flag IPIN_MSGRDY is set and the message is further inspected. If the message is an ICMP echo request, it is automatically serviced. If the message contains a UDP frame, the flag UDPIN_MSGRDY is set. In any case, message information such as source and destination addresses, message header and data length, etc. are written to variables stored in external RAM to be accessible to the application.

As stated, NetApi51 is UDP oriented. Typically the application is interested only in the data portion of a UDP message. The function NetGetUdpMsg() is provided for this purpose. The function receives a pointer to a character buffer, to which it copies the message. The size of the message is returned by the function. Note that if the UDPIN_MSGRDY flag is set and the function NetGetUdpMsg() returns zero, it means that a UDP message with no data was received. Similarly, if the function is called when no UDP message is ready (UDPIN_MSGRDY flag zero), the function simply returns zero.

Once the UDP message is retrieved, the application may obtain information about the message by several NetApi51 functions. Of course, the message is now copied into internal RAM, and the application may find the frame contents by inspecting the message, but it is more convenient to call the provided functions.

NetGetUdpInSrcEthernAddress(char *pcSrcEther) copies the sender's ether address to the character array pcSrcEther.

NetGetUdpInSrcIpAddress(char *pcSrcIP) copies the sender's IP address (source IP) to the character array pcSrcIP.

NetGetUdpInSrcPort() returns the source UDP port.

NetGetUdpInDestPort() returns destination UDP port

If the application requires other information, such as IP flags, or IDs, it must inspect the message frame now copied into external RAM. Please refer to the section titled "Frame Access" below for more information.

A.3.3 Message Transmission

Frames to be transmitted are composed in external RAM. The low-level view of a transmit operation consists of two steps. First, the network driver chip is informed of a transmit request, along with the size of the frame. The network driver chip uses local memory to store frames to be transmitted. The chip grants the request only when there is enough room in its local memory to hold the frame. Then, the frame is copied from external RAM to the local memory of the driver chip. The driver chip transmits the message, which may require waiting for the medium to be available, or even retransmitting it if collision occurs. The driver chip is polled to see if the frame has successfully been transmitted.

Again, being UDP-oriented, NetApi51 provides a straightforward means of transmitting UDP messages. The function NetSendUdpMsg() takes two arguments. The first is a pointer to the character buffer holding the message. The second is the number of characters (bytes) to transmit. It composes the frame, computes the checksums, asks the driver chip for permission to transmit, copies the frame to the driver chip, and finally waits for the transmission to be completed. It returns an error code, zero if successful, non-zero if there were errors in transmission.

Before NetSendUdpMsg() is called, several parameters of the UDP message must be set. Namely, the destination ether address and IP address, and the source and destination ports. The source ether and IP addresses previously specified during initialization are used. The following functions set the parameters of the UDP message to be transmitted.

```
NetSetUdpOutDestEthernAddress(char *cEther)
NetSetUdpOutDestIpAddress(char *cIP)
NetSetUdpOutSrcPort(int nDestPort)
NetSetUdpOutDestPort(int nSrcPort)
```

Both cEther and cIP are pointers to character arrays holding the ethernet and IP address of the destination.

A.3.4 Frame Access

Low-level frame access is available as the incoming messages are placed in a buffer. This buffer, referred to as the receive buffer, is kept in external data memory. A pointer to this memory may be declared and the buffer contents be accessed as array elements. Note that the buffer is an external variable to the C

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code. Similarly, the external variable `E_MSGRDY` is nonzero when an ethernet message is placed in the receive buffer. Its size is stored by the external variable `EIN_SIZE`. The following code portions illustrate the use of these variables.

```
extern int E_MSGRDY, EIN_SIZE, RX_BUFFER;
char c, *RxBuffer;

// check incoming IP messages
if(!E_MSGRDY) continue;

RxBuffer=&RX_BUFFER;

c=RxBuffer[12]; // get the 12-th byte of the message
```

Alternatively, the receive buffer elements may be accessed as two-byte integers. The function `SwapEndian()` interchanges the two bytes of its integer argument. It is convenient in translating network integers (with high byte first) to C integers (with low byte first).

```
int n, *RxBuffer;
RxBuffer=&RX_BUFFER;

n=RxBuffer[12]; // get the 12-th integer (bytes 24 and 25)
n=SwapEndian(RxBuffer[12]);
```

A.3.5 Serial I/O Function

The serial input/output functions are collected in the library `xSio51.lib`. Its source code is available. It is a generalization of the `Sio51`, `cSio51`, and `csSio` libraries. The library contains the usual functions `putc()`, `getc()`, and `peekc()`.

The functions `puts()` and `cputs()` transmit the strings given by their arguments. The function `puts()` assumes that the string is in external data memory, while `cputs()` assumes that the string is in code memory.

The same applies to the functions `printf()` and `cprintf()`. The latter assumes the format string is in code memory, while the former assumes it is in external data memory.

Stream support is provided by the two functions `sprintf()` and `csprintf()`. Here, the first argument is the stream (character buffer) into which the formatted strings are written. In either case, the stream is assumed to be in external data memory (it is not possible to write to the MCS-51 code memory). Again, `sprintf()` assumes that the format string is in external data memory, while `csprintf()` assumes that the format string is in code memory.

The library contains the initialization function `InitSerialPort0(int nMode)`. The function

```
unsigned int GetCodeWord(unsigned int uAddress);
```

is used by the code-memory-versions of the functions to read the MCS-51 code memory. The argument is the address in code memory.

A.4 HARDWARE ISSUES

A.4.1 Hardware Overview

The CS8900A is connected to the microcontroller in the manner recommended by the manufacturer (see references 1 and 3). The CS8900A is operated in the so-called "I/O Mode" (see reference 2 and 5). The I/O Mode registers of the CS8900A are memory-mapped into the microcontrollers external data memory starting at address 0xFD00. This address is determined by the CPLD equations of the Xilinx 95C36. Note that the CS8900A cannot generate interrupts, support DMA or use an EEPROM when running in the 8-bit mode (see reference 4).

A.4.2 Communicating with the CS8900A Ethernet Driver

The eight I/O Mode registers of the CS8900A are memory-mapped to the external data memory of the microcontroller, starting at address 0xFD00. Note that the CS8900A registers are 16-bit registers. Thus, the CS8900A I/O Mode register space occupies the external data memory block 0xFD00 to 0xFD0E of the microcontroller. A write operation is accomplished in two steps. First, the target address is written to the "PacketPage Pointer" register of the CS8900A. Then the data is written to the "PacketPage Data" register of the 8900A. The read operation similarly follows this two-step procedure. The address is written to the "PacketPage Pointer" as in the write operation. The data is read from the "PacketPage Data" register. Care must be taken to read and write both bytes in the required order (see reference 4).

The following code illustrates the data flow interface between the microcontroller and the CS8900A.

```
#define CS8900A_BASE      0xFD00

; -----
; input  : word address in [r3:r2]
CS8900A_SetPacketPagePtr:
    mov    dptr, #(CS8900A_BASE+0x0A)
    mov    a, r2
    movx   @dptr, a
    mov    dptr, #(CS8900A_BASE+0x0B)
    mov    a, r3
    movx   @dptr, a
    ret

; -----
; input  : word address in [r3:r2]
; input  : data word in [r1:r0]
CS8900A_PutWord:
```

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```
    lcall CS8900A_SetPacketPagePtr
    mov   dptr, #(CS8900A_BASE+0x0C)
    mov   a, r0
    movx  @dptr, a
    mov   dptr, #(CS8900A_BASE+0x0D)
    mov   a, r1
    movx  @dptr, a
    ret

; -----
; input  : word address in [r3:r2]
; output : data word in [r1:r0]
CS8900A_GetWord:
    lcall CS8900A_SetPacketPagePtr
    mov   dptr, #(CS8900A_BASE+0x0D)
    movx  a, @dptr
    mov   r1, a
    mov   dptr, #(CS8900A_BASE+0x0C)
    movx  a, @dptr
    mov   r0, a
    ret

; -----
```